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## Flip Chip Integration Technology

### Flip-Chip Technology Enables:

- High I/O interconnection density and low lead inductance.
- Active-Passive component integration on a variety of platforms, e.g., composite substrates, PCBs, etc.
- Hybrid integration for Multi-system functionality On-Chip.
- 3-D Through-wafer interconnects for optical computing applications (e.g. Micro-Optical Interconnects).

### Desired Properties For A Flip Chip Process:

- High placement accuracy for high density interconnections.
- A low temperature process with simplistic fabrication steps.
- Reworkability of solder for extra degree of freedom with die attach.
- Lead-free, environmentally safe materials.

### Acknowledgements

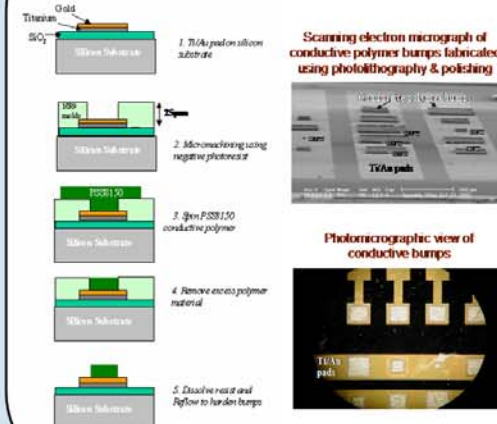
This work is supported by the Army Research Laboratory through the Composite Materials Technology program.

## Conductive Polymer Technology

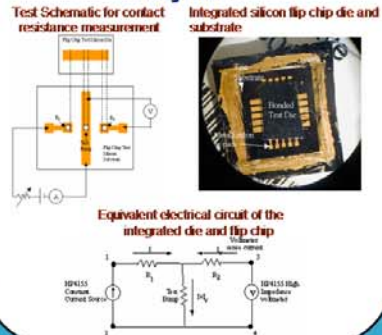
### Salient Features:

- Low temperature wafer bumping process using conventional semiconductor processing techniques (photolithography & polishing).
- Lead-free, reworkable (thermoplastic) and offers simpler processing steps.
- Screen and squeegee-free process with greater bumping resolution than industrial processes (~1-2mm as against ~10mm for screens).
- Obviates expensive metal deposition steps otherwise used in conventional wafer bumping processes.
- Offers accurate control over bump size and height (can fabricate application-specific high-aspect ratio bumps).

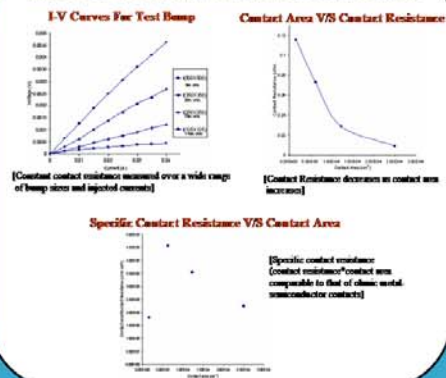
## Wafer Bumping Process



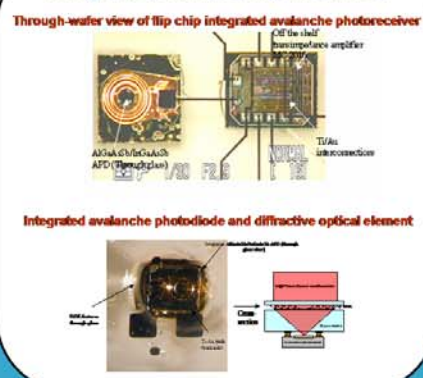
## Contact Resistance Measurements for Conductive Polymer



## Electrical Characterization Results



## Integrated Multi-Chip Modules



## Characterization Results For Integrated MCMs

